In the Specification:

Please replace the last paragraph on page 7 continuing onto page 8 with the following amended paragraph:

FIG. 4 is a partial cross-sectional view of semiconductor substrate **100** after a planarization process and illustrates non-uniform planarization of fill layer **150**. In FIG. 4, a planarization process has been performed. Planarization processes include CMP and fixed abrasive grinding. In second region **140**, the planarization processes removed all fill layer **150** from above top surface **125A** of silicon nitride layer **120** leaving a top surface **160A** of fill layer **150** in second region **140** and top surface **125A** of silicon nitride layer **120** substantially co-planer. In first region **130**, a thickness H5 of fill layer **150** remains above top surface **125** of silicon nitride layer **120** and a top surface **160B** of fill layer **150** in first region **130** and top surface **125** of silicon nitride layer **120** therefore not planer. Note that top surface **125A** is lower than top surface **125** by a distance H6 since silicon nitride layer [[**125**]] **120** is used as planarization stop layer and some over polish/over grinding is performed. In a CMP process, a polishing stop layer functions because it is harder than the material be removed and is abraded away slower, is more resistant chemically to the etchant (if any) contained in the polishing slurry or both. In a fixed abrasive grinding process, a grinding stop layer functions because it is harder than the material be removed and is abraded away slower.